

Notice of Allowability

Application No.

09/482,332

Examiner

Fred Ferris

Applicant(s)

LAMSON ET AL.

Art Unit

2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 28 May 2004.
2. ☒ The allowed claim(s) is/are 1-3 and 9-33.
3. ☒ The drawings filed on 14 January 2000 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached:
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

JEAN R. HOMERE
PRIMARY EXAMINER

DETAILED ACTION

1. *A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 28 May 2004 has been entered. Claims 1-3 and 9-33 are currently pending in this application. Claims 4-8 have been cancelled by applicants. Claims 1-3 and 9-33 have now been allowed over the prior art of record.*

Response to Arguments

2. *Applicant's arguments filed 28 May 2004 have been fully considered and found to be persuasive.*

Regarding applicant's response to 112(1) rejection: *The examiner withdraws the 112(1) rejection in view of applicant's arguments and submission of articles relating to the structuring of the analysis generator filed 28 May 2004.*

Regarding applicant's response to 103(a) rejection: *The examiner withdraws the 103(a) rejection in view of applicant's amendment to the claims and arguments filed 28 May 2004.*

Allowable Subject Matter

3. *Claims 1-3 and 9-33 have been allowed over the prior art of record.*

The following is an examiners statement of reasons for allowance:

Applicants are disclosing a computer based system and method for modeling an electronic device (IC) structure by electrical simulation and analysis of semiconductor packages. The method includes the elements (generator/integrator) and steps for input characteristics of a package/structure model as segments, subdivisions, and compositions, sequenced elements for analysis, electrically analyzing segments, integrating the analysis into a single model, and creating a specific model format. These features are generally disclosed in the prior art (see U.S. 5,694,344 (Yip et al) Fig. 7, and Righi et al pp. 1907-1909 (Section III), for example) However, the prior art of record, while generally disclosing these features, does not meet the conditions as suggested in MPEP section 2132, namely:

*"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an **ipsissimis verbis** test, i.e., identity of terminology is not required. **In re Bond**, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."*

In this case, the prior art of record does not disclose the specific sequence of steps and arrangement of elements (see Figs. 2-5) as disclosed within the context of independent claims 1, 12, and 22. These steps and elements relate to:

A system and computer-implemented method for modeling an electronic package/structure comprising:

- Input generator: steps of – acquiring data describing model characteristics of segments, subdivisions and compositions, coupled to:*

- Segmentation generator: steps of - selecting, organizing, storing, converting segments of modeled structure into segment file,
coupled to:
- Analysis generator: steps of - analyzing segment file in calculation programs creating output file,
coupled to:
- Integrator: steps of - integrating output file into single model file and storing,
coupled to:
- Output generator: creating summary file files in specific format.

The closest prior art of record uncovered during examination discloses various methods of computer implemented interconnect simulation and modeling of semiconductor substrate packaging. For example:

U.S. Patent 5,694,344 issued to Yip et al discloses designing physical layout of an IC package and selecting interconnect segments but does not disclose the analysis process coupled with integration process of the claimed invention.

U.S. Patent 5,371,390 issued to Mohsen discloses designing physical layout and interconnection of an IC package directed to use in hybrid circuits and multichip modules. Mohsen also discloses the use of horizontal and vertical segmentation but does not teach converting, analyzing, or integrating the resulting segment files.

U.S. Patent 6,499,004 issued to Huber et al discloses designing physical packages for electronic components and includes an input system (Input Data Generator) for inputting physical design characteristics and an analysis program but does not teach segmentation of conductors in an electronic structure.

Claims 2-3, 9-11, 13-21, and 23-33 are deemed allowable as being dependent from independent claims 1, 12, and 22 respectively.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.*

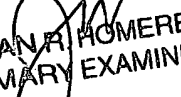
Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.

The Official Fax Numbers are:

Official -(703)-872-9306

Fred Ferris, Patent Examiner
Simulation and Emulation, Art Unit 2128
U.S. Patent and Trademark Office
Crystal Park 2, Room 2A22
Crystal City, Virginia 22202
Phone: (703) 305 - 9670
FAX: (703) 305 - 7240
Fred.Ferris@uspto.gov

September 2, 2004


JEAN R. HOMERE
PRIMARY EXAMINER